application in advance of any other application, including "special" applications, except for reissues involved in "litigation", and treat and respond to all issues immediately.

In The Specification:

Please replace the paragraph beginning at column 1, line 64, and ending at column 2, line 11 with the following paragraph:

Figs.4A shows an example of the scanning line driving circuit **250**. The scanning line driving circuit **250** includes clocked [invertor] inverter used circuits **410** to **412** (as shown in Figs.4B), NAND circuits **403** and **404** and [invertor] inverter type buffers **405** and **406**. The clocked [invertor] inverter used circuit includes clocked invertors **420** and **421** operated by using a clock signal CK (as shown in FIG.4C) and an invertor **422**. The start pulse signal which synchronizes a vertical synchronizing signal is input from a start pulse signal input terminal **402**, and the clock pulse signal which synchronizes the horizontal synchronizing signal is input from a clock pulse signal input terminal **401**. Therefore, the scanning lines are driven sequentially through scanning line connection terminals **407** and **408**.

In The Claims:

Please amend claims 3, 6 , 8, 12, 13, 14, 18, 19, 24 and 26 as follows.

a1

3. (Amended) The device of claim 1 wherein the number of pixel electrodes equals [to] the number of the digital memory circuits [circuit].

a2

6. (Amended) An active matrix display device having an electro-optical modulating layer disposed between a pair of substrates [substrate], said active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

a thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said thin film transistor, wherein said memory circuit stores an information output by said thin film transistor; and

a2 cont.

at least two voltage source [signal] lines electrically connected to said memory circuit [and the corresponding pixel electrode],

wherein different voltages are applied to said pixel electrode through said at least two voltage source [signal] lines based on the information stored by the corresponding memory circuit; and

wherein said memory circuit comprises a pair of inverters connected to each other, each of said inverters comprising an N-channel TFT and a P-channel TFT.

a3

8. (Amended) The active matrix display device of claim 6 wherein the number of pixel electrodes equals [to] the number of the digital memory circuits [circuit].

12. (Amended) An active matrix display device having an electro-optical modulating layer disposed between a pair of substrates [substrate], said active matrix display device comprising:

a4

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

a first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor, wherein said memory circuit stores an information output by said first thin film transistor; and

at least two voltage source [signal] lines electrically connected to said memory circuit [and the corresponding pixel electrode],

wherein different voltages are applied to said pixel electrode through said at least two voltage source [signal] lines based on the information stored by the corresponding memory circuit, and

wherein said memory circuit comprises at least second and third thin film transistors, one of source or drain of the second thin film transistor being connected with one of said voltage source [signal] lines, a gate electrode of the third thin film transistor, and one of source or drain of the first thin film transistor,

the other of source or drain of the second transistor being connected with the other of said voltage source [signal] lines and one of source or drain of the third thin film transistor, and

a gate electrode of the second thin film transistor being connected with the other of source or drain of the third thin film transistor, one of said voltage source [signal] lines, and said [electro-optical modulating layer] pixel electrode,

wherein said active matrix display includes a time gradation display device.

a4 concl.

13. (Amended) The active matrix display device of claim 12 wherein a voltage supplied to the [the] electro-optical modulating layer is substantially zero on time average.

14. (Amended) The active matrix display device of claim 12 wherein the number of pixel electrodes equals [to] the number of the memory circuits [circuit].

15. Canceled

16. Canceled

a5

18. (Amended) An active matrix display device having an electro-optical modulating layer disposed between a pair of substrates [substrate], said active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

a first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor, wherein said memory circuit stores an information output by said first thin film transistor; and

a5 cont.

at least two voltage source [signal] lines electrically connected to said memory circuit [and the corresponding pixel electrode],

wherein different voltages are applied to said pixel electrode through said at least two voltage source [signal] lines based on the information stored by the corresponding memory circuit, and

wherein said memory circuit comprises at least two [invertors] inverters, said [invertors] inverters comprising at least two thin film transistors and being connected with said voltage source [signal] lines.

19. (Amended) The active matrix display device of claim 18 wherein the number of pixel electrodes equals [to] the number of the memory circuits [circuit].

24. (Amended) An active matrix display device having an electro-optical modulating layer disposed between a pair of [substrate] substrates, said active matrix display device comprising:

a6

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

a first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor, wherein said memory circuit stores an information output by said first thin film transistor; and

at least two voltage source [signal] lines electrically connected to said memory circuit [and the corresponding pixel electrode],

a6 and

wherein different voltages are applied to said pixel electrode through said at least two voltage source [signal] lines based on the information stored by the corresponding memory circuit, [and]

wherein said memory circuit comprises at least two thin film transistors, having a same conductivity type, and

wherein said active matrix display device includes a time gradation display device.

a7 26. (Amended) The active matrix display device of claim 24 wherein the number of pixel electrodes equals [to] the number of the memory circuits [circuit].

28. Canceled.

Please add the following new claims.

47. The active matrix display device according to claim 6 wherein said electro-optical modulating layer comprises a liquid crystal.

a8 48. The active matrix display device according to claim 12 wherein said electro-optical modulating layer comprises a liquid crystal.

49. The active matrix display device according to claim 18 wherein said electro-optical modulating layer comprises a liquid crystal.

50. The active matrix display device according to claim 24 wherein said electro-optical modulating layer comprises a liquid crystal.

51 An active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by a substrate and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said substrate;

a switching element disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said switching element, wherein said memory circuit stores an information output by said switching element and comprises a pair of inverters, each of said inverters comprising an N-channel TFT and a P-channel TFT,

wherein different voltages are applied to said pixel electrode based upon information stored by corresponding one of said memory circuit.

A8 concl.

52. A method of operating an active matrix display device comprising the steps of:

storing a data in a memory circuit provided at one pixel;

supplying a voltage to a pixel electrode of said pixel in accordance with the data stored in said memory circuit;

applying an AC voltage to an opposite electrode opposed to the pixel electrode,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

53. The method according to claim 52 wherein said voltage applied to the pixel electrode is output by said memory circuit.

54. The method according to claim 52 wherein said active matrix display device is a liquid crystal display device.